Remarks

Applicant respectfully requests reconsideration of the rejection of the claims in view of the claim amendments above and the remarks set forth below. Claims 1-20 remain in the application. Claims 1-20 were previously presented.

35 U.S.C. §103

Claims 1 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakai et al. (US 6,247,034)in view of Park et al. (US 6,470,030). In order to support a prima facie case of obviousness under 35 U.S.C. § 103(a), each and every element of the claim must be shown in the references cited. The applicants respectfully propose neither Nakai nor Park, taken individually or in combination, show all of the elements of claim 1.

Independent claim 1 recites, inter alia, an "Orthogonal Frequency Division Multiplexing (OFDM) receiver . . . comprising . . . a shared buffer that stores data corresponding to the OFDM signals . . . a processor that is adapted to receive data from the shared buffer, perform computations on the data and return data to the shared buffer . . . an equalizer module adapted to receive data from the shared buffer and equalize the data . . . and **a receiver controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module.**" (Emphasis added).

The "receiver controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module" is an important element of the claimed invention. More specifically, the "receiver controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module" element overcomes the shortcomings of the conventional buffer arrangement of using a separate buffer associated with each functional block. The conventional buffer arrangement and shortcomings are described as follows on page 3, lines 1-5 of the application:

> The functional blocks or modules of OFDM receivers are typically connected in series so that the output of one functional block goes into a buffer associated with the next functional block. This arrangement takes up space and increases the processing overhead associated with processing OFDM signals. A buffer architecture that avoids these shortcomings would be desirable.

In other words, the "receiver controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module" element of claim 1 overcomes the shortcoming of the conventional buffer arrangement used in OFDM receivers since a plurality of separate buffers between functional blocks is not used. Rather in the inventive arrangement, one shared buffer is used by all of the functional blocks and access to the shared buffer is controlled by the controller.

Nakai appears to be directed towards an FFT processing unit containing a single processing element, a butterfly operation unit, connected to two RAM memory units under control by a controller unit (FIG. 1; Col. 8, ln. 30 to col. 9, ln. 27). The RAM memory units are dedicated for the operation of the butterfly operation unit. Nakai does not appear to show or suggest that the RAM memory units are shared with additional processing elements or that the controller controls how the butterfly operation unit and additional processing elements access the RAM memory units. Indeed, as acknowledged in the October 28, 2008 office action, independent claim 13 does not disclose "a device controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module" element. Applicants' respectfully note that independent claim 1 recites a similar "receiver controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module" element that is not disclosed by Nakai.

Park appears to be directed towards an OFDM receiver having a rearrangement memory connected in series between an FFT processor and a synchronizing section (FIG. 1; Col. 3, lns. 44-56). The October 28, 2008 office action states that Park (fig. 1, Controller 570, FFT processor 710 and the Equalizer element 600, col. 64? To col. 4, line 8) discloses a "controller that controls access to the shared buffer by the processor and controls the transfer of data from

the shared buffer to the equalizer module." Applicants respectfully disagree. Park appears to teach a controller 570 that receives data from a synchronizing section 540 and controls synchronization and phase error estimation based on the data received from the synchronization section 540. (Col. 3, line 64 to col. 4, line 8). To control synchronization and phase error estimation the controller 570 appears to perform feed back control of the rotator 510 and A/D converter 500. (Col. 9, line 39 to col. 10, line 4; Col. 10 line 53 to col. 11, line 11). Park does not appear to teach a buffer being shared by the equalizer element 600 and the processor 710 let alone the controller 570 controlling access to the shared buffer by the by the equalizer element 600 and processor 710. Indeed, Fig. 1 of Park appears to only show connection lines between the controller 570 and the synchronization section 540, A/D converter 500, and rotator 510 and there does not appear to be any connection between the various memories shown in Fig. 1 and the controller 570.

In contrast to Nakai and Park, claim 1 recites "a shared buffer that stores data corresponding to the OFDM signals...a processor that is adapted to receive data from the shared buffer, perform computations on the data and return data to the shared buffer...an equalizer module adapted to receive data from the shared buffer and equalize the data... and **a receiver controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module.**" Neither Nakai nor Park, individually or in combination, show or suggest the "receiver controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module" element of amended claim 1. Indeed, Nakai and Park appear to merely illustrate the conventional buffering arrangement discussed in the background of the application (page 3, lns. 1-5). As discussed above, the claimed "receiver controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module" element of amended claim 1 overcomes the shortcomings of the conventional buffering arrangement. As a result, it is respectfully proposed that the rejection for obviousness under 35 U.S.C. § 103(a) is overcome and notice to that effect is earnestly solicited.

Dependent claims 2-12 being dependent on and further limiting independent claim 1, should be allowable for that reason, as well as for the additional recitations that they contain. Applicant respectfully requests reconsideration of the rejection of the claims in view of the above amendments and remarks.

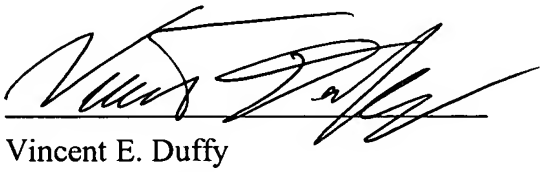
Independent claim 13 is contains elements similar to independent claim 1 and should be allowable for the reasons discussed above. Therefore, it is respectfully proposed that the rejection for obviousness is overcome.

Dependent claims 14-20 being dependent on and further limiting amended independent claim 13, should be allowable for that reason, as well as for the additional recitations that they contain. Applicant respectfully requests reconsideration of the rejection of the claims in view of the above remarks.

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the Applicants' attorney at (818) 480-5223, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fees, other than those discussed above, are believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,



By: Vincent E. Duffy
Reg. No. 39,964
Phone (818) 480-5223

Patent Operations
THOMSON Licensing LLC
P.O. Box 5312
Princeton, New Jersey 08543-5312
April 28, 2009

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I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

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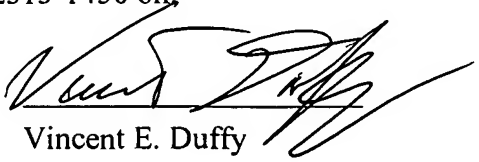

Vincent E. Duffy

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PATENT OPERATIONS

MAILING TO U.S. Patent and Trademark Office

Docket No PU020354 Serial No. 10/523,442 Filed: 1/31/05 Patent No. _____

Inventor(s): Maxim Borisovich Belotserkovsky Atty: Vincent E. Duffy

Title: Centralized Buffer Architecture For an OFDM Receiver

APPLICATION AS FILED									
Enter Date	Enter Number		Check Type		Check Items Mailed with Application				
		Independent Claims		Original-US Nat'l	☐	Declaration			
		Claims in Excess 20	☐	Divisional	☐	Statement under CFR § 1.56-013M			
		Claim Pages	☐	Continuation	☐	Assignment & Recordation Sheet			
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		Abstract Pages	☐	Re-Exam	☐	IDS 1449 with References			
			☐	US Provisional		Utility Application Transmittal	Express Mail Application Label No.:		
	Charge		☐			Fee Transmittal Sheet in duplicate	Date Deposited: 4/28/09		
Mailed	Due	AMENDMENTS	Mailed	Due	APPEALS	Mailed	Due	FEES	
		After Rejection			Notice of Appeals			Filing Fee Exp.	
4/28/09	1/28/09	After Final Rejection			Appeal Brief			Issue Fee	
	[redacted]	After Allowance U/R312			Reply Brief	4/28/09		RCE Fee	
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		Statement DOE		[redacted]	Claim Disclaimer		[redacted]	Letter to PO	
		Statement under §1.56			Status Letter		[redacted]	Notif. of Foreign Ref.	
		IDS w/_____ references			Declaration			Correction Of Record	
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